REMARKS

This is in response to the Office Action dated January 27, 2006. Claims 1-3 and 5-23 are pending.

Claim 1 stands rejected under 35 U.S.C. Section 102(b) as being anticipated by Ooishi (US 2002/0057111).

Ooishi in Fig. 2 discloses an alleged first stage including PMOS transistors 40-41 and NMOS transistors 42-43, and an alleged second stage including PMOS transistors 53-54 and NMOS transistors 55-56. The first stage is allegedly a logic operation circuit. The latch portion of the former stage includes PMOS transistors 44, 46 and 47 and NMOS transistors 45, 48 and 49, whereas the latch portion of the latter stage includes PMOS transistors 51, 53, 54 and NMOS transistors 52, 55, 56. The Office Action contends that the "first cell" of claim 1 is made up of transistors 41, 42, and that the "second cell" is made up of Ooishi's latch portion of the latter stage including transistors 53-56. The Office Action contends that by turning on transfer gate 50, data is transferred from the latch portion of the alleged first stage to the latch portion of the alleged second stage (see paragraph 0039).

The Section 102(b) rejection of claim 1 is respectfully traversed for at least the following reasons.

Claim 1 requires that the *second cell functions as a driver circuit for driving the first cell (or the logic operation circuit)*. Ooishi fails to disclose or suggest this feature of claim 1. The Office Action contends that this is met due to signal TG2B. However, TG2B is generated by a non-illustrated control circuit synchronizing with the basis clock signal (see paragraph 0037). In other words, TG2B is not generated by the second cell or stage. Thus, the alleged second stage

in Fig. 2 of Ooishi does not function as a driver circuit for driving the alleged first stage. For this reason, the Section 102(b) rejection of claim 1 lacks merit.

It is noted that according to Ooishi, "[t]he TG1 signal and the TG1B signal are signals generated by the control circuit (not shown) synchronizing with a basic clock signal (not shown) . . . The TG2 signal and the TG2B signal are signals also generated by the control circuit synchronizing with the basic clock signal." See paragraph [0037] of Ooishi. Thus, Ooishi makes clear that TG2B is not a feedback signal of the latch portion of the latter stage as apparent alleged in the Office Action, because TG2B is generated by the control circuit for synchronizing with the basic clock signal which is not shown. Thus, Ooishi fails to disclose or suggest at least that the second cell functions as a driver circuit for driving the logic operation circuit as recited in claim 1.

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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